Design and Development of FPGA system for RADAR applications

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Abstract— Digital Filters play a vital role in various types of signal processing applications. It is the key performance of the filters, which made DSP so popular. Such filters have two important roles to play: signal separation and signal restoration. When a signal is buried in the noise, then filter performs signal separation. On the other hand, signal restoration done by the filter when they are distorted. The main objective of this paper is that Field programmable gate arrays (FPGA) digital filters implemented and to present an easy device for different applications. Digital filters have superior performance over analog signal processing. There are two types of digital filters: infinite impulse response (IIR) and finite impulse response. (FIR).The main function of FPGA based digital filters is to capture the features in the signal and to eliminate the noise from the signal coming from the space. The accurate value of wind velocity, particle density, velocity measurement etc for meso sphere, stato sphere, and tropo sphere (MST) radar is very important. For Radar (Antennas), the operating frequency is also very important to transmit power into free space. DSP based FPGA system shows superior performance to achieve good operating frequency and to filter the noise effectively for the signal. This is required for radar applications. The high operating frequency (more than MHz) is obtained by FPGA based signal processing rather than by DSP floating or fixed point processors.

Index Terms— FPGA, DSP, Processors, Radar, MST, Digital filters, IIR, FIR, Xilinx and Altera.

1 INTRODUCTION

FPGAs can provide a high performance alternative to DSP processors. The present trend is the implementation of digital filters using application specific integrated circuits. This trend has completely changed the scenario of digital filtering by means of improved sampling rate and speed of computation. FPGAs are used to eliminate some of the problems associated with the custom approach. The most of FPGA architectures are system programmable and configurations of the device may be changed at the implementation level. The DSP- FPGA is configured to perform the specialized soft ware functions required for radar signal processing. Even it is possible to change the device with out extensive hardware modifications, so that memory and time can be saved.

VHDL programs have developed to implement digital filters by FPGAs: Xilinx and Altera. This implementation technique is going to propose to implement at radar centre. Signal processing system in Radar requires speed which is related to clock frequency and accuracy is related to word length, area related to hard ware and power related to energy.Digital filters are more effiecient to obtain good signal to noise ratio than analog filters. The main demerit of analog filter is that noise is added to the signal at each intermediate stage. Digital filter performs noisless mathematical operations at each stage in the transform.

This digital filtering is one of an important aspect to process the signals received by the antennas. The radar antennas have two functions: to transmit and receive the signal. It transmits the signal into MST spheres to detect the wind velocity, particle density and etc. After detecting the signal in the free space it reflect back to the antenna receiver and it transforms to the system to process the signal digitally. In this aspect implementation of digital filters are very important to capture the features contained in the signal and

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to remove the noise in the signal.As the digital filters have emrged as a strong and good option for removeng noise, shaping the signal and spectrum, and minimizing the inter-symbol interference in communication technology. This can be achieved by FPGAs efficiently rather than DSP processors.

2 HARD WARE ARCHITECTURE

Optimal architecture for a particular application involves trade-offs between area, performance, and response. The abudance of dedicated MAC (Multiply-Accumulate) blocks in the FPGA devices present the option for implementing either an area efficient "serial" or high-performance "parallel" digital filters. Serial architectures share a single MAC resource, making it an area efficient but at the expense of performance, because one clock- cycle is required for each tap delay register. This architecture is an excellent choice for area sensitive, low-performance applications.High-performance, high-order filtering applications that are able to exploit dedicated multiplier or DSP blocks, often turns to FPGAs for a solution. By replicating the multiply-adder logic once for each tap delay register, the entire filtering calculation can be performed in a single clock cycle.FPGA device with dedicated DSP blocks capable of supporting cascaded "multiply-add" operations such as the Xilinx/Altera has the highest performance is achieved using a "transposed" architecture. Utilizing the same resources as "direct" form digital filters, data samples are applied in parallel to all tap multipliers through pipeline registers. The products are then applied to a cascaded chain of registered adders, combining the effect of accumulators and registers.

Direct form archtecture for IIR

$Y(n) = b0x(n)+b1x(n-1)+------+bMx(n-M)-a1y(n-1)-a2(n-2)-…..an(n-N)-------1$

Where b_i and a_j filter coefficients and N and M are the filter length.

The above equation is said be FIR filter when $a_j = 0$

In direct form 2 structure N=M , so memory saved.

Transposition theorem states that if you reverse the directions of all branch transmittances and interchange the input and output in the flow graph [3]. The input and output properties of the transfer function remain unchanged.

The above equation states that multipliers, adders and memory elements are required to implement digital filter.

3 FPGA FOR DIGITAL FILTER IMPLEMENTATION

In the present work with different FPGA devices and numbers, digital (IIR and FIR) filters are implemented with and with out pipe lining for different orders. Pipe line is defined as fetching the next instruction to the processor while the current instruction executes. The pipe line is used intensively to improve the performances of the system. The main function of the pipe line is that multiplication is divided into number of small steps. This means that less circuitry between clock steps which in turn mean that clock run at faster rate and over all performance of the processor increases. Digital filter are implemented using techniques: direct form and Transpose form

For most DSP applications the data rate is much more important than any latency. Latency is the number of cycles between the executions of two consecutive instructions on the same function unit. Therefore the critical path of pipe line implementation of nth order for digital filter structure is reduced. One extra cycle is needed to latch the input and n cycles are required to shift the first input to the last tap for nth order filter. In this work Altera and Xilinx are used. The programs have developed for FPGAs Altera: Mercury, statix, etc and Xilinx's: Spartan and vertex for various lengths of digital filters have exhibited a very good operating frequency response and stability.

This fast expansion in number of gates per device has made all the difference for radar systems integrators and their signal processing systems providers.

The maximum speed is achieved using the architecture consists of multipliers and adders unlike other scholars who avoided multipliers. Avoiding multipliers lead to the

requirement of different code which consumes time. In this present work normal soft ware is used and maximum speed is achieved.

The sample code to implement the shifting of registers is given below (example for IIR)

X0 ≤Xi latching the input

For I 1 in 7 loop

X (i) ≤ X (i-1)

For I 2 to 7 loop

Y (i) ≤ Y(i-1)

End loop

For FIR we have only one type of coefficients.

4 RESULTS

The maximum operating speed is obtained in the present work by implementing pipe-line technique. Higher operating frequency obtained due to optimization of critical path for transposed form of filter. Under the case studies made on the devices of FPGAs Altera and Xilinx, results shows that the Xilinx series have exhibited superior performance while the Mercury series of Altera have exhibited faster response. We compared the results obtained by both FIR and IIR and shows that FIR filters have got high speed due to pipe line but latency is the problem. Where as IIR are executes at faster rate than FIR but phase is the problem. It is clear that the implementation of pipelining and reduce the order of the filter increase the frequency which helps the signal processing more reliable and decrease the time factor for radar applications. For low order filter decrease the operating frequency but the signal quality improves. Table 1 shows for IIR filter, Mercury series of FPGA got maximum operating frequency and when we implement filter by means of pipeline, the maximum operating frequency is still improved. Mercury series of Altera has got nearly 200 MHz frequency with pipe line for 8th order. Table 2 shows for FIR filter Altera device has got higher operating frequency than Xilinx device. The higher operating is achieved by implementing pipe line for FIR filters of both Altera and Xilinx devices. Maximum operating frequency means less time period takes to execute the instructions. This is more important aspect especially in signal processing. In this paper we focused on pipe line to improve frequency and there by reducing time period to execute the mathematical expressions. For Xilinx the operating frequency is around 350 MHz. The research work done with the IIR and FIR filters for the signal processing by FPGA devices for different lengths of orders got good operating frequency than general purpose processors. Further it is clear that the pipe line architecture of FPGA increases the operating frequency so that time period also reduced. Therefore the digital filters with FPGA technology are very useful and more efficient to capture the features and filter the noise in the signal to process the signal for radar applications.

Table1.Implemetation of IIR filter for pipeline

Device name	Frequency (MHz) for 4th order	Frequency(MHz0 for 8th order
Flex 10ke	58	48
Cyclone	164	154
Mercury	227	193
Startix	156	135

Table 2. Implementation of FIR filters for 8 taps

Device name	Frequency (MHz) for 8 taps
Vertex	349
Spartn3	320
Mercury(Altera)	400
Cylone(Altera)	460

5 CONCLUSIONS

In the present work, Implementation of digital filters

by FPGA device shows superior performance than DSP processors with respect to frequency, time and filtering of the signal. FIR filter shows better results than IIR filters to get good operating frequency and better phase.FPGAs get more sophisticated, performing and integrating more DSP blocks and it is becoming the standard and more efficinet. FPGA devices consume less power than General purpose processors. The configuration files for FPGA can be stored or generated as and when required and downloaded into FPGA to reconfigure them.Thereofre it is more advantage for remote user. As FPGAs increase in density and performance capability, more signal-processing functions can be incorporated to the radar system for filtering and signal correlation. Integrating DSP functions into a single FPGA, the system-level reduced in size, weight and power.Thus FGPGA based signal processing is best suitable for radar applications to capture the features and eliminate the nise in the signal to get accurate wind velocity, particle density,etc from the the sapce(atmospheric data).

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